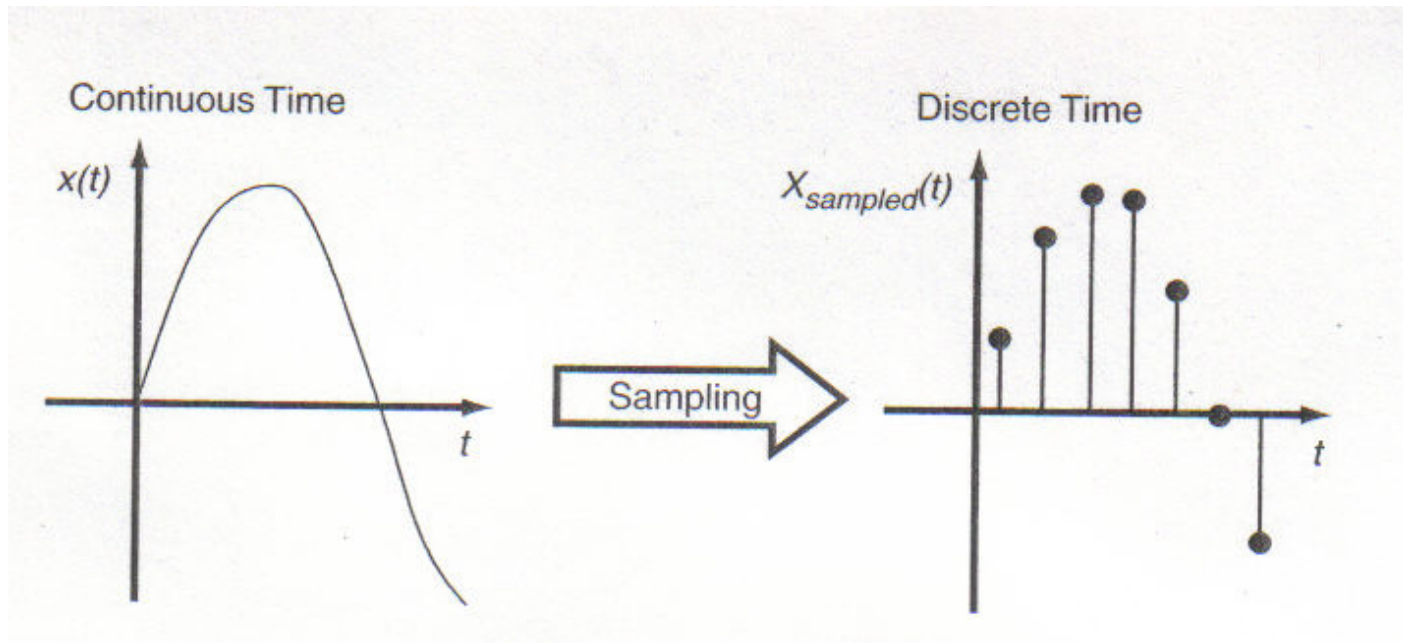


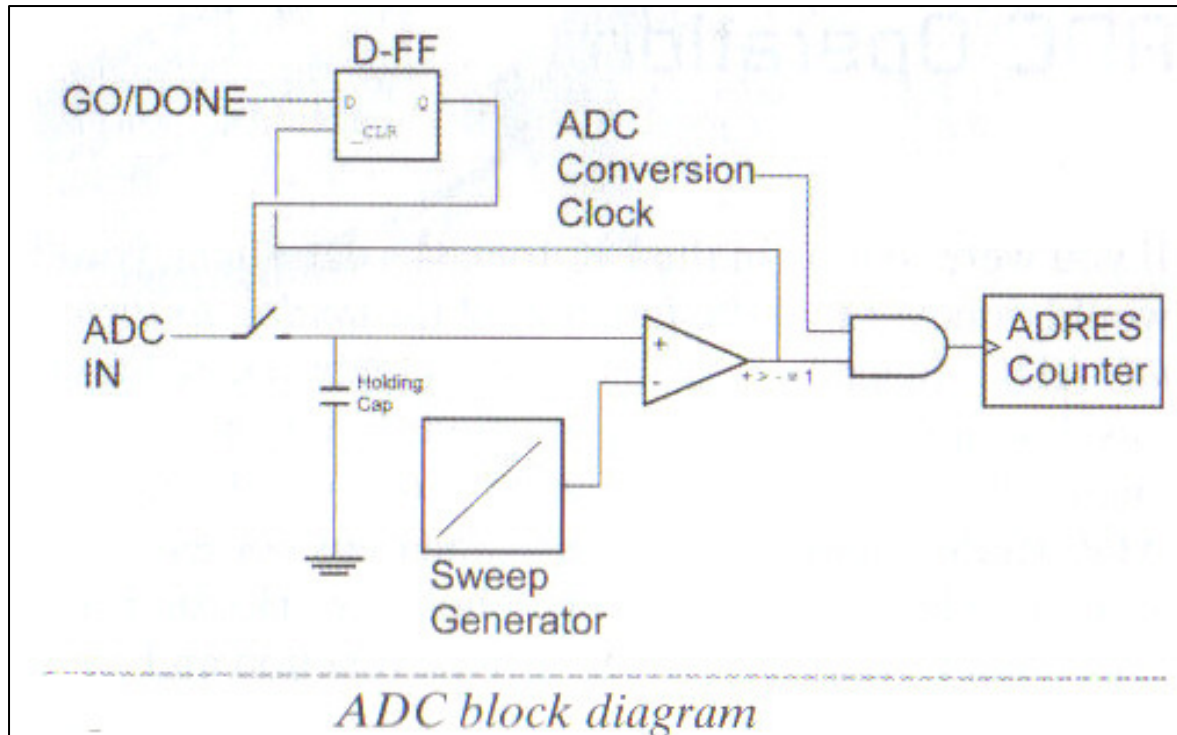
Using ADC

A/D Process



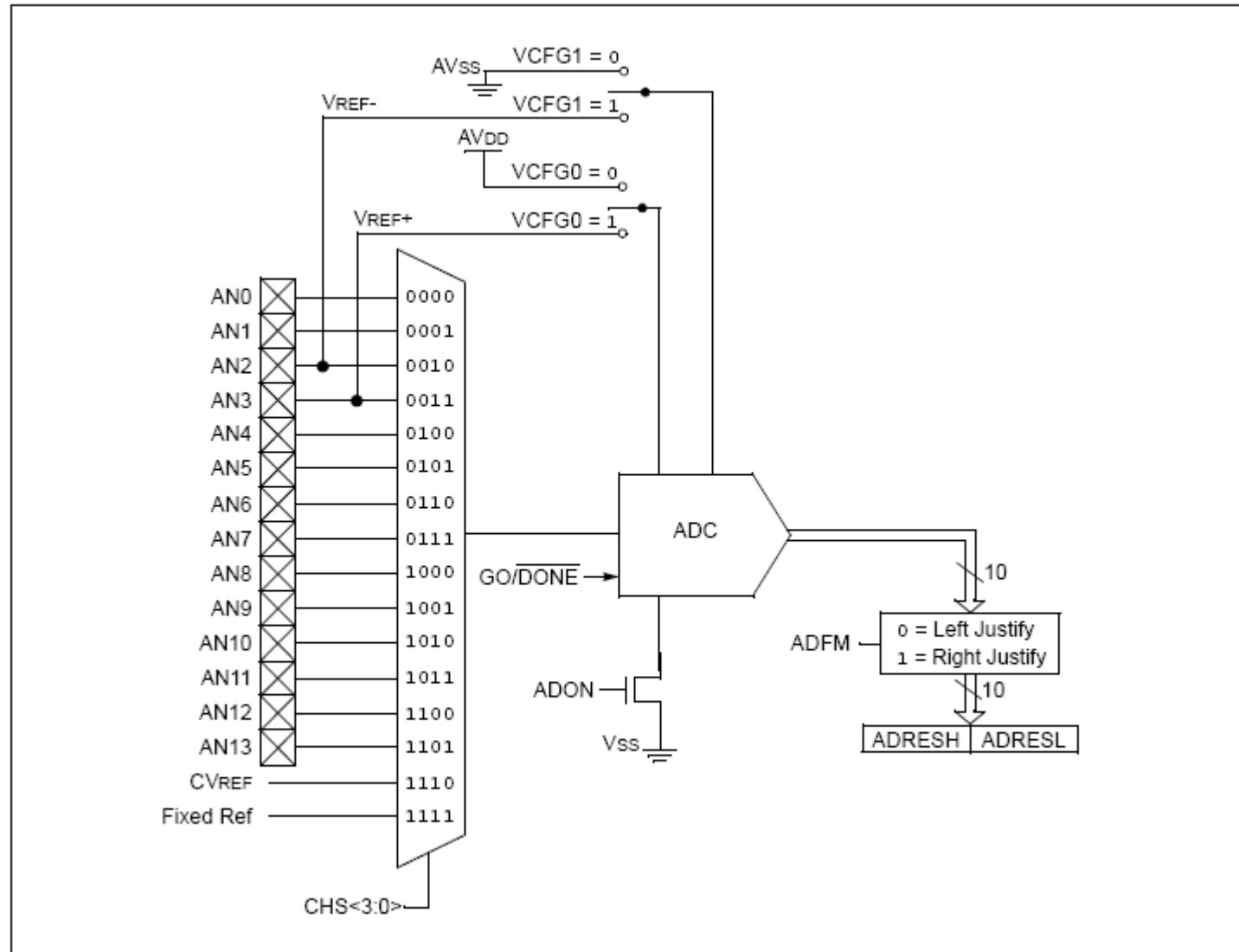
Critical to measuring external sensor inputs for control and monitoring

ADC Block Diagram



16F887 ADC Block Diagram

FIGURE 9-1: ADC BLOCK DIAGRAM



Description

- The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog
 - Inputs, which are multiplexed into a single sample and hold circuit.
 - The output of the sample and hold is connected to the input of the converter.
 - The converter generates a 10-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESL and ADRESH).
 - The ADC voltage reference is software selectable to be either internally generated or externally supplied.
 - The ADC can generate an interrupt upon completion of a conversion.
- Interrupts can be used to wake-up the device from Sleep.

ADC Configuration

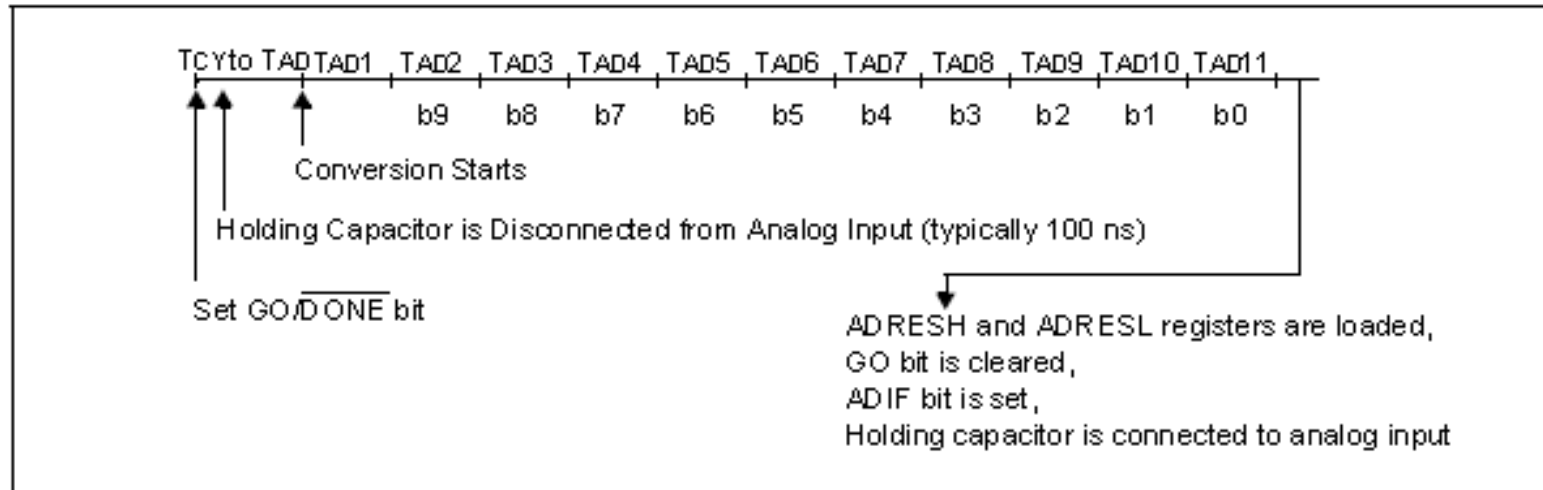
- When configuring and using the ADC the following functions must be considered:
 - Port configuration
 - Channel selection
 - ADC voltage reference selection
 - ADC conversion clock source
 - Interrupt control
 - Results formatting

ADC Configuration

- Port Configuration
 - When converting analog signals, the I/O pin should be configured for analog by setting the associated TRISA and ANSEL bits.
- Channel selection
 - ADCON0 register determine which channel is connected to the sample and hold circuit.
- ADC VOLTAGE REFERENCE
 - VCFG bits of the ADCON0 register
- CONVERSION CLOCK
 - ADCS bits of the ADCON1 register
 - Note: The time to complete one bit conversion is defined as TAD. One full 10-bit conversion requires 11 TAD periods
- Results formatting
 - ADFM bit of the ADCON0

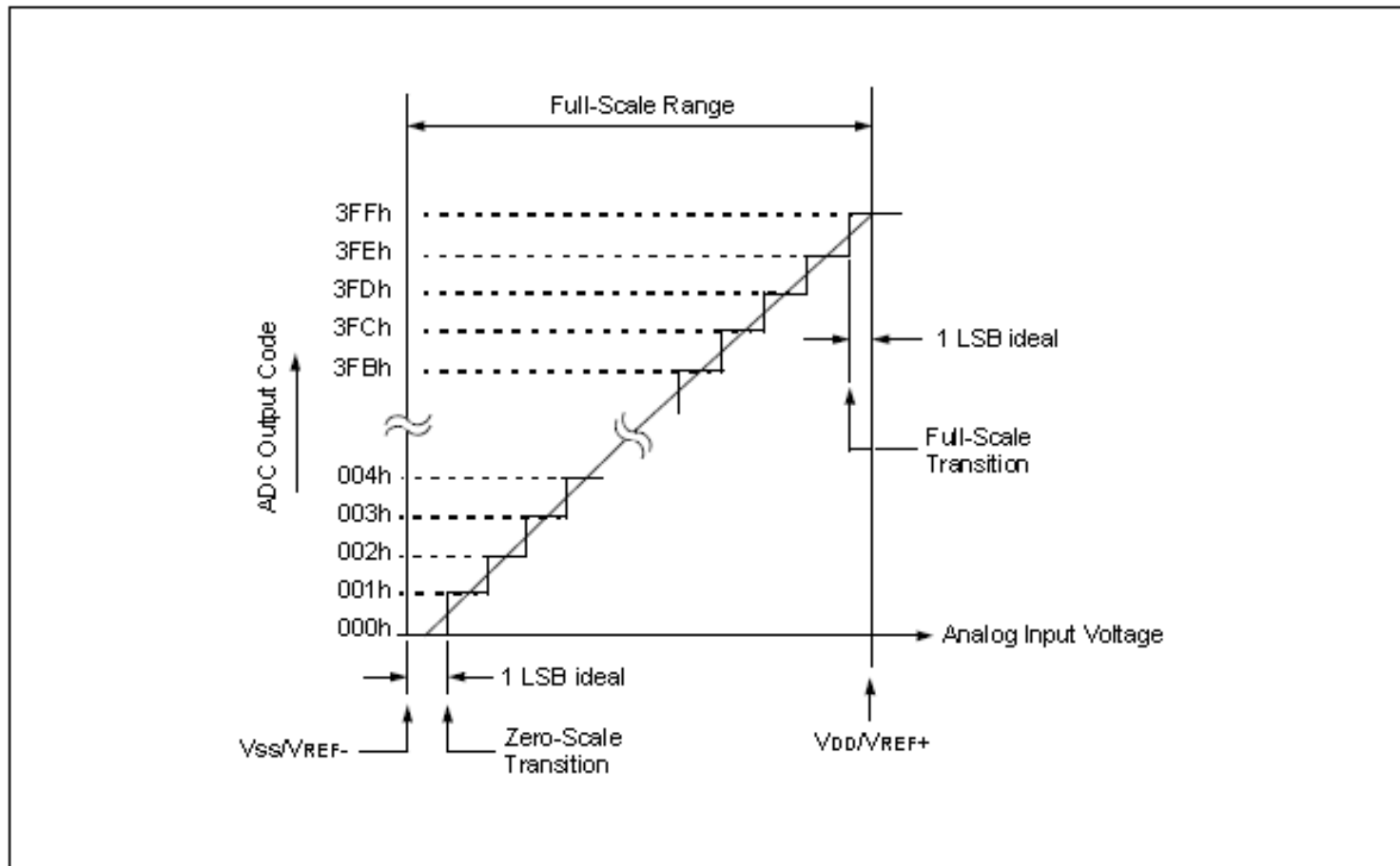
10 bit Conversion Process

FIGURE 12-2: ANALOG-TO-DIGITAL CONVERSION T_{AD} CYCLES



Transfer Function

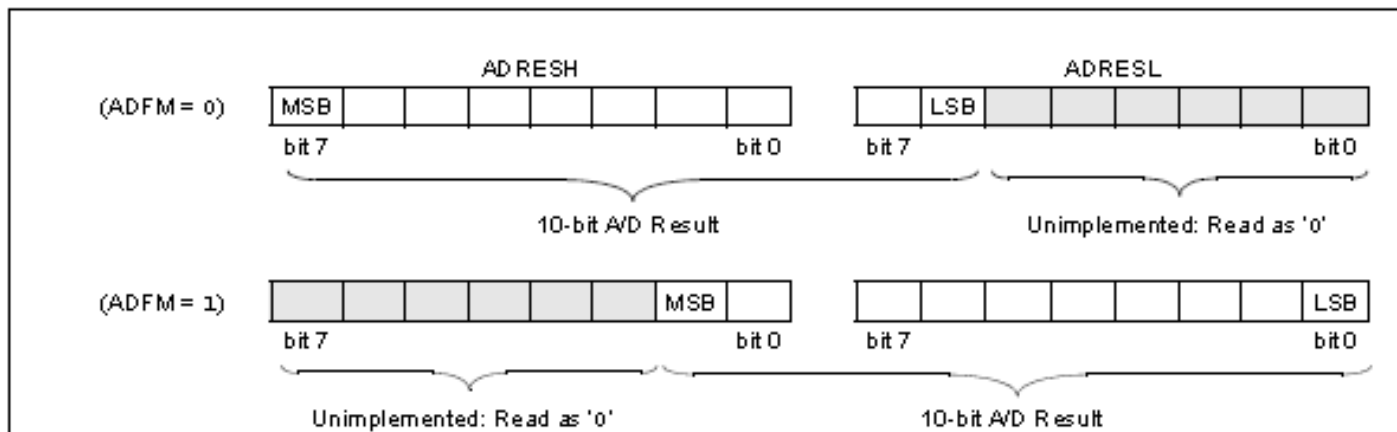
FIGURE 12-5: ADC TRANSFER FUNCTION



Result Formatting

- The 10-bit A/D conversion result can be supplied in two formats, left justified or right justified.
- The ADFM bit of the ADCON0 register controls the output format.

FIGURE 12-3: 10-BIT A/D CONVERSION RESULT FORMAT



ADC Conversion

- **STARTING A CONVERSION**
 - To enable the ADC module, the ADON bit of the ADCON0 register must be set to a '1'.
 - Setting the GO/DONE bit of the ADCON0 register to a '1' will start the Analog-to-Digital conversion.
- **COMPLETION OF A CONVERSION**
 - When the conversion is complete, the ADC module will:
 - Clear the GO/DONE bit
 - Set the ADIF flag bit
 - Update the ADRESH:ADRESL registers with new conversion result

ADCON1

REGISTER 3-1: ADCON1: A/D CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
ADFM	—	VCFG1	VCFG0	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

- bit 7 **ADFM:** A/D Conversion Result Format Selection bit
 1 = Right justified
 0 = Left justified
- bit 6 **Unimplemented:** Read as '0'
- bit 5 **VCFG 1:** Voltage Reference bit
 1 = VREF- pin
 0 = Vss
- bit 4 **VCFG 0:** Voltage Reference bit
 1 = VREF+ pin
 0 = VDD
- bit 3-0 **Unimplemented:** Read as '0'

ADCON0

REGISTER 3-2: ADCON0: A/D CONTROL REGISTER 0

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS1	ADCS0	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 7-6 **ADCS<1:0>**: A/D Conversion Clock Select bits
 00 = FOSC/2
 01 = FOSC/8
 10 = FOSC/32
 11 = FRC (clock derived from a dedicated internal oscillator = 500 kHz max)

bit 5-2 **CHS<3:0>**: Analog Channel Select bits
 0000 = AN0
 0001 = AN1
 0010 = AN2
 0011 = AN3
 0100 = AN4
 0101 = AN5
 0110 = AN6
 0111 = AN7
 1000 = AN8
 1001 = AN9
 1010 = AN10
 1011 = AN11
 1100 = AN12
 1101 = AN13
 1110 = CVREF
 1111 = Fixed Ref (0.6 volt fixed reference)

bit 1 **GO/DONE**: A/D Conversion Status bit
 1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
 This bit is automatically cleared by hardware when the A/D conversion has completed.
 0 = A/D conversion completed/not in progress

bit 0 **ADON**: ADC Enable bit
 1 = ADC is enabled
 0 = ADC is disabled and consumes no operating current

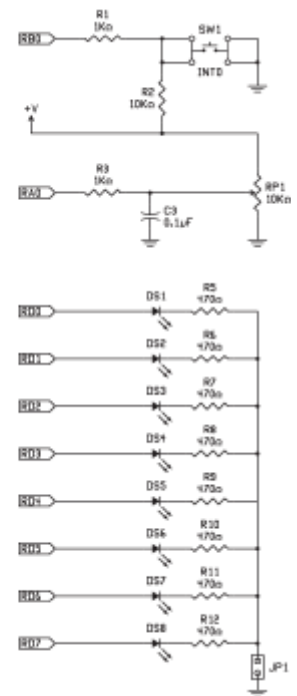
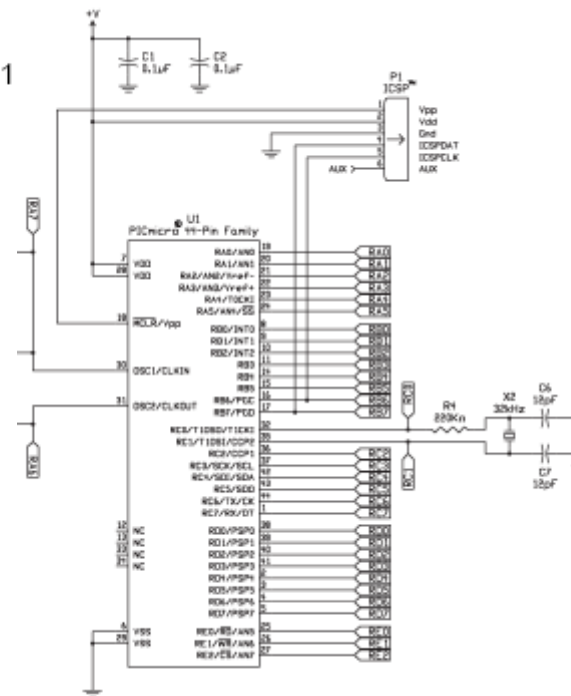
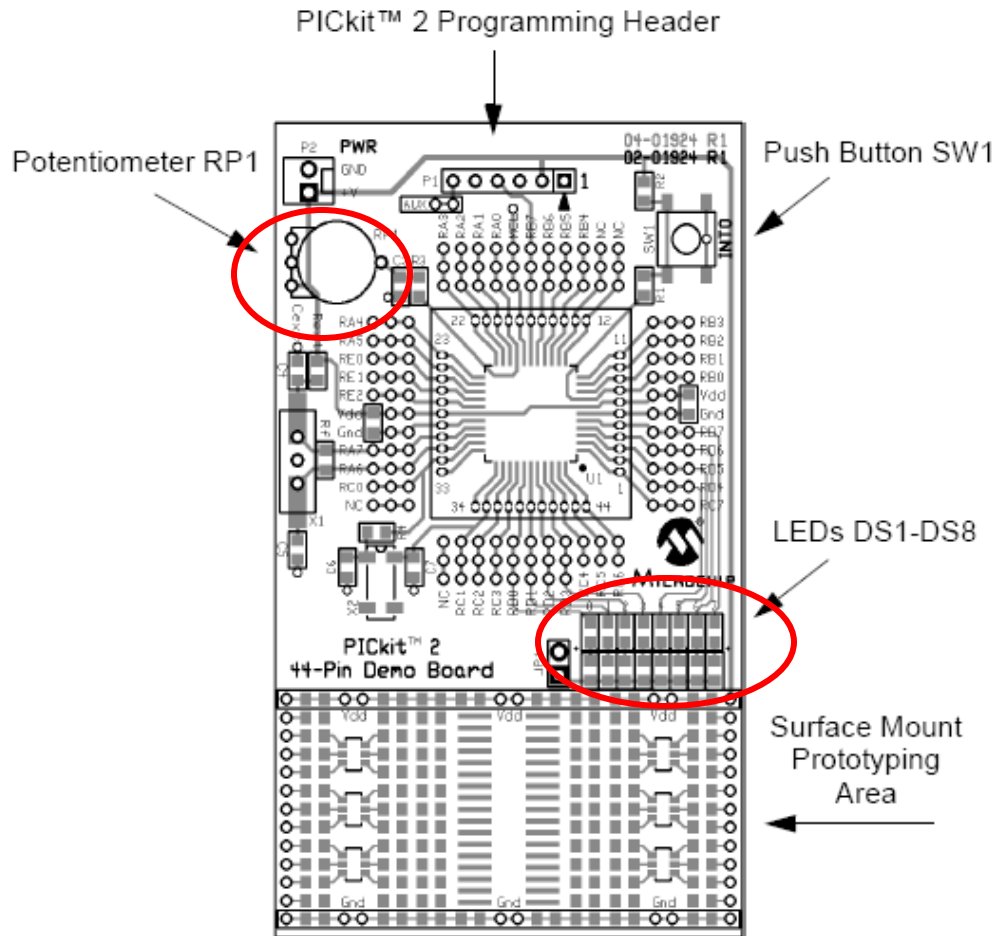
ADC Exercise Overview

- For purposes of this lesson, the ADC must be turned on and pointed to channel AN0 on pin RA0.
- The ADC needs about 5 μ s, after changing channels, to allow the ADC sampling capacitor to settle.
- We can start the conversion by setting the GO bit in ADCON0. The bit also serves as the DONE flag. That is, the ADC will clear the same bit when the conversion is complete.
- The answer is then available in ADRESH:ADRESL.
- This lesson takes the high order 8 bits of the result and copies them to the display LEDs attached to PORTD.

ADC Code

- Component parts
 - Initialization
 - TRISA
 - ANSEL
 - ADCON0
 - ADCON1
 - Continuous Loop
 - Delay
 - Update PORTD
 - State machine for ADC Conversion and retrieval of data from ADRESH

44 Pin Demo Schematic and Layout



Exercise

- Navigate to C:\EET250\16F887\Lesson 7 ADC with Demo Board\adc and Open project ADC.mcp
- You need to add code in places indicated to
 - Configure ADCON0
 - Configure ADCON1
 - Configure TRISA
 - Configure ANSEL
- Compile code
- Download and execute. Move pot from one extreme to the other
- Note ADC output is updated on Ports LED as pot input is adjusted
- If error then Set breakpoint at ADCValue = ADRESH and configure watch for ADRESH. Adjust pot to difference setting is ADRESH changing.
- If it isn't recheck your SPR configurations
- If problem persists check solutions folder.